REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-18 are now present in this application. Claims 1 and 13 are independent. Claims 1 and 13 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Rejection Under 35 U.S.C. § 112, 1st Paragraph

Claims 1-18 stand rejected under 35 U.S.C. § 112, 1st Paragraph. This rejection is respectfully traversed.

The Examiner states that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It appears that the Examiner has assumed that the gate line, data line and drain are shorted together via the pixel electrode. With regard to claim 1 (as amended), a gate line, a data line and a drain is not mentioned. Further it is clear that the input line part cannot be a data line, a gate line or a drain because neither of these provide signals to driver ICs. With regard to claim 13, (similarly amended), connectivity in the cell is distinguished from connectivity

in the input line part.

As set forth in the Applicants' claim 1, the pixel electrode connects first, second and third line layers together in the line input part. While the pixel electrode (and the other lines) may form a common layer with the corresponding layer in the cell array region at some point during a manufacturing process, claim 1 does not recite such connectivity. In fact, the input line side is isolated from the cell array side, direct connectivity being broken by the data or gate driver ICs. A multi-layer input line part formed of different metals provides a variable resistive path, thus addressing the stated problem of retarded drive resistance. It is convenient to form the layers on the input line side at the same time they are formed on the cell array side. However, as shown in Figs. 6D and 7D, respectively, the pixel electrode does not maintain connectivity between the input line side and the cell array side. Short-circuiting between the two sides is neither claimed, nor illustrated, nor intended by the Applicants.

Based on the reasons set forth above, Applicants respectfully submit that the claims as recited and amended herein, are fully supported by and adequately described in the written description of the invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Rejection Under 35 U.S.C. § 112, 2nd Paragraph

Claims 13-18 stand rejected under 35 U.S.C. § 112, 2nd Paragraph. This rejection is respectfully traversed.

The Examiner has set forth certain instances wherein the claim language is not clearly understood.

In order to overcome this rejection, Applicants have amended claim 13 to correct each of the deficiencies specifically pointed out by the Examiner. Further, the Applicants submit that simultaneous formation of corresponding layers on a line input side and a cell array side facilitates ease of manufacturing.

Applicants respectfully submit that the claims, as amended, particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Obviousness-Type Double Patenting Rejection

Claims 1-18 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-14 of U.S. Patent No. 6,466,280 to Park, in view of U.S. Patent No. 6,528,357 to Dojo et al. (Dojo) and U.S. Patent Application 2002/0101398 to Fujita. This rejection

is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

The Applicants respectfully submit that the Examiner has not met the initial burden of establishing a prima facie case of obviousness. Foremost, it is well-established law that in order to establish a prima facie case of obviousness, *inter alia*, the prior art references (or references when combined) must teach or suggest all the claim limitations. In this case, none of the cited references teach or suggest *all of the limitations* of independent claims 1 and 13, as amended.

In this regard, independent claim 1 has been amended to recite a combination of elements in an LCD device having an input line part, including a pixel electrode on the passivation layer to electrically connect the first, second and third line layers through each contact hole, said first, second and third line layers providing signals to driver ICs, said driver ICs applying output signals to gate lines or data lines.

Independent claim 13 has been similarly amended to recite a combination of steps in a method for manufacturing an LCD device having a cell array region and an input line part, including forming a pixel electrode on the passivation layer to electrically connect to the drain electrode of the cell

array region and to connect the first, second and third line layers through the contact holes in the input line part, said first, second and third line layers providing signals to driver ICs, said driver ICs applying output signals to said gate line or said data line.

The Applicants respectfully submit that these combinations of elements are not disclosed or suggested by the prior art of record, including Park, Dojo and Fujita.

In making this rejection, the Examiner has particularly stressed the Park patent as covering claims 1 and 13, and also states that the limitations for the input line (electrodes) arrangement for an LCD device are covered by claims 8-14 of Park. The Examiner's position rests on a premise that *the input line part can be any signal input lines such as gate lines or data lines*. However, in view of the current amendments to independent claims 1 and 13, this premise must be set aside.

Particularly, the data lines and gate lines are located in the cell array region of the LCD, and as such, they do not provide signals to driver ICs. Therefore, since these and other similar elements mentioned by the Examiner are located downstream of the driver ICs, they do not meet the Applicants' claimed combinations including *said first, second and third line layers providing signals to driver ICs, said driver ICs applying output signals to gate lines or data lines*. Neither does elements located on the cell array region of Dojo or Fujita

teach or suggest this feature, because the asserted elements do not provide signals to driver ICs.

Hence, the above-recited references do not teach or suggest the Applicants' claimed combinations, and therefore the Examiner has not met the initial burden of establishing a prima facie case of obviousness.

With regard to dependent claims 2-12 and 14-18, Applicants submit that claims 2-12 and 14-18 depend, either directly or indirectly, from independent claims 1 and 13, which are allowable for the reasons set forth above, and therefore claims 2-12 and 14-18 are allowable based on their dependence from claims 1 and 13. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone

Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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